REMARKS

The Examiner is respectfully requested to reconsider and withdraw the objection to claims 8 and 21 for the following reasons.

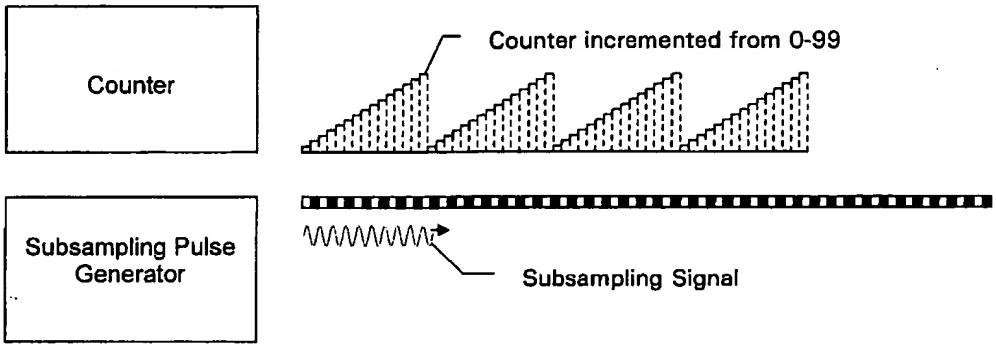
Claim 8 requires the following steps:

"applying the sub-sample clock signals to a counter;

resetting the counter with the sample clock signals; and

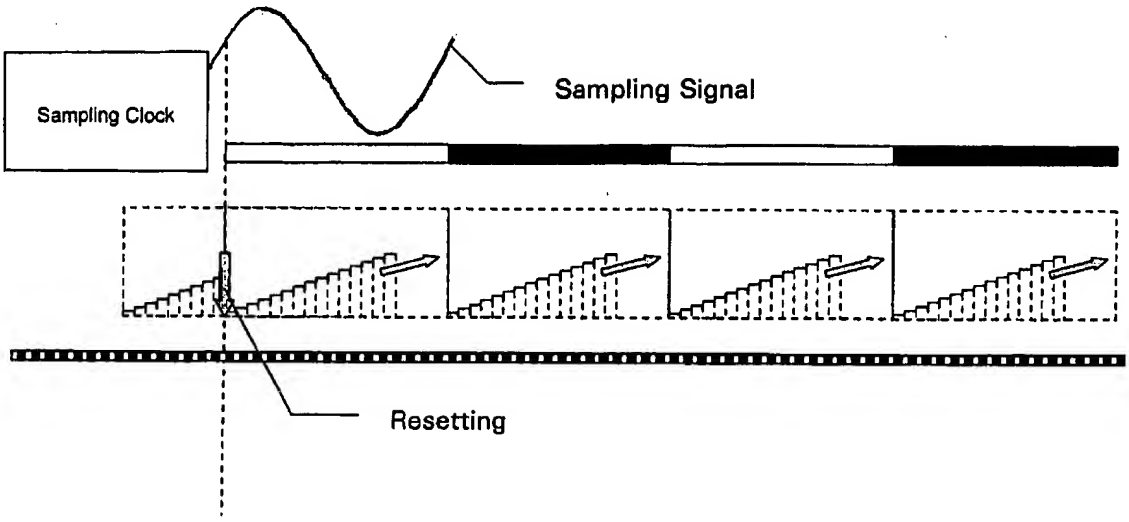
using the counter value as the measure of clock phase."

It is apparent that this, when read on Applicants' specification, is fully supported. Figure 17 shows the components of the system. Sub-sample clock signals are applied to a counter which is thereby driven and periodically incremented from 0 to 99.



Therefore, the sub-sampling clock and the counter are synchronous as they are driven by the same signal. Each numeric count within a cycle from 0-99 corresponds to a period of the sub-sampling signal and to the sub-sample clock. Without resetting, there is no correlation to the sampling signal.

In the next step, the counter is reset by the sample clock signal, i.e., set to a starting condition representing Zero.



Due to the resetting of the counter – triggered by the sampling signal – the numeric value of the counter and the sampling signal or the sampling clock are now running synchronously. Each of the counter's values represents a definite subdivision of the sampling signal or clock phase. Therefore, it is possible to use the counter values as the measure of the clock phase. Thereby, the counter provides a finer resolution of the clock phase by subdividing each sampling interval. Due to the triggering by the sample clock, the counter is correlated and synchronous. Thus, the counter provides a measure of the clock phase recited in claim 8.

Claim 8 requires resetting the counter with the sample clock signal to begin counter incrementation, with the counter being clocked by the sub-sample clock signal. Thus, the count or measure of the counter is a representation of clock phase of the clock signal, as recited in claim 8. Note that while the clock produces a number representing phase, it is reset each time the phase value is equal to Zero, and thus the output of the counter is always representative of the phase of the clock. The claim 6 recitation that the measure of clock phase is derived from sub-sample clock signals is consistent with the claim language since the sub-sample clock signal produces a count which represents the phase of the clock signal.

The above comments also equally apply to claim 21. Simply stated, the clock phase count is derived using the sub-sampling clock signal to produce a count representative of the phase of the clock signal. Thus, the measure of clock phase of the clock signal is derived from the sub-sample clock signal but a measure of the clock phase of the clock signal.

In view of the foregoing, reconsideration and withdrawal of the Examiner's objection and allowance of all claims is respectfully requested.

In the event the Examiner is not persuaded to allow the claims for the reasons set forth herein, the Examiner is respectfully requested to contact the undersigned to further discuss the objection and try to arrive at an acceptable compromise to overcome the Examiner's concerns.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: May 19, 2006

Respectfully submitted,

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